



An ASIC Low Power Primer: Analysis, Techniques and Specification

By Rakesh Chadha, J. Bhasker



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This book provides an invaluable primer on the techniques utilized in the design of low power digital semiconductor devices. Readers will benefit from the hands-on approach which starts from the ground-up, explaining with basic examples what power is, how it is measured and how it impacts on the design process of application-specific integrated circuits (ASICs). The authors use both the Unified Power Format (UPF) and Common Power Format (CPF) to describe in detail the power intent for an ASIC and then guide readers through a variety of architectural and implementation techniques that will help meet the power intent. From analyzing system power consumption, to techniques that can be employed in a low power design, to a detailed description of two alternate standards for capturing the power directives at various phases of the design, this book is filled with information that will give ASIC designers a competitive edge in low-power design.

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Bibliography

- Sales Rank: #1919500 in Books
- Brand: Brand: Springer
- Published on: 2012-12-05
- Original language: English
- Number of items: 1
- Dimensions: 9.21" h x .56" w x 6.14" l, 1.11 pounds
- Binding: Hardcover
- 218 pages

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Editorial Review

From the Back Cover

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- Starts from the ground-up and explains what power is, how it is measured and how it impacts on the ASIC design process;
- Provides essential information in an easy to read and understand format, using basic examples;
- Explains what power intent is, how to describe it precisely and what techniques can be used to achieve the power intent with the two key standards, the Unified Power Format (UPF) and Common Power Format (CPF).

About the Author

J. Bhasker is a well-known expert in the area of hardware description languages and RTL synthesis. He has been chair of two working groups: the IEEE 1076.6 VHDL Synthesis and the IEEE 1364.1 Verilog Synthesis and was awarded the IEEE Computer Society Outstanding Contribution Award in 2005. He is an architect at eSilicon Corporation responsible for the timing of many complex designs.

Rakesh Chadha is a CAE and Design Professional with over 25 years experience, including 18 years in project leadership and technical management. He was responsible for the timing and signal integrity for the Sematech project on Chip Parasitic Extraction and Signal Integrity Verification. He is Director of Design Technology at eSilicon Corporation and is responsible for complex SOC design methodology.

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